REMARKS

Claims 41-67 are pending in the present application.

In the office action mailed April 24, 2003 ("the Office Action"), claims 41-43, 45-48, and 54-62 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,363,382 to Tsukakoshi ("the Tsukakoshi patent") in view of Hancu *et al.*, A Concurrent Test Architecture for Massively Parallel Computers and Its Error Detection Capability, IEEE Transactions on Parallel and Distributed Systems, Vol. 5, No. 11, Nov. 1994 pp. 1169-84 ("the Hancu article"). Claims 44, 49-53, and 65-67 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of the Hancu article in further view of U.S. Patent No. 4,652,793 to Meaden ("the Meaden patent"). Claims 44, 49-53, and 65-67 were also rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of the Hancu article in further view of U.S. Patent No. 5,659,737 to Matsuda ("the Matsuda patent"). Claims 44, 49-53, and 65-67 were further rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of the Hancu article in further view of IBM technical disclosure bulletin entitled, Improved Hash and Index Searching Techniques for Computers Using a Cache And/Or Virtual Memory, June 1, 1988 ("the IBM technical disclosure).

Claim 41 is patentable over the Tsukakoshi patent in view of the Hancu patent because the combined teachings of these references do not teach or suggest the combination of limitations recited in claim 41. Claim 41 recites a method for accessing a memory, comprising comparing a memory address of a memory access request to decompressed defective memory addresses that are otherwise stored in a compressed format, the defective memory addresses having substitute addresses associated and stored therewith, where the memory address matches one of the decompressed defective memory addresses, extracting the substitute address associated therewith, and accessing a memory location corresponding to the extracted substitute address rather than a memory location corresponding to the memory address.

As discussed in the Applicant's previously filed responses, there are at least two reasons for the rejection of claim 41 under 35 U.S.C. 103(a) must be withdrawn. First, the Examiner's characterization of the teachings of the Tsukakoshi patent and the Hancu patent are inaccurate. Second, even if it is assumed that the Examiner's characterization of the Tsukakoshi

patent and the Hancu patent were accurate, for the sake of argument, the references, either alone or in combination, do not teach or suggest the combination of limitations recited by claim 41.

The Examiner has characterized the Tsukakoshi patent as teaching "comparing memory addresses for a fault memory analysis (access/test) by performing substitute address allocation (mapping or remapping) and provides compression means in col. 2 lines 35-50." *See* Office Action pp. 1-2. However, the Examiner's characterization of the Tsukakoshi patent is inaccurate, and overly broad. As mentioned in the previously submitted responses, the Tsukakoshi patent teaches a system and method for exploiting an inherent characteristic of the design of redundant memory in a memory device which enables the use of a fault analysis memory (FAM) having a capacity that is less than that of the memory under test (MUT). More specifically, the Tsukakoshi patent teaches using a single cell in the FAM to represent "n" redundant rows or columns where n redundant rows or columns are replaced each time a redundant memory repair is made in the memory device. From the failure data stored by the FAM, a redundancy solution is calculated in order to resolve remapping of defective memory locations to redundant memory locations.

A thorough reading of the Tsukakoshi patent, which the Examiner is suggested to do, will clearly show that "comparing memory addresses for fault memory analysis (access/test) by performing substitute address allocation" is not disclosed anywhere in the Tsukakoshi patent. As explained in some detail in Applicant's previously submitted responses, there is no comparison of any memory addresses. It appears that the Examiner has failed to recognize the difference between "memory addresses" and the *data* stored by *a memory location* corresponding to a memory address. The Tsukakoshi patent describes comparing the *data* read from a memory location to expected *data* in order to find defective memory cells, which is well known. However, the *memory addresses* are not being compared. That is, the binary value that is provided to a MUT to identify a memory location to be tested is not compared with any other value.

Moreover, the Examiner's characterization that the Tsukakoshi patent compares memory addresses for fault analysis "*by* performing substitute address allocation (mapping or remapping)" (emphasis added) does not make any sense. That is, allocating substitute addresses does not mean, or even imply, that memory address are compared for fault analysis. Consider

that if addresses were to be substituted, how is it that any fault analysis is ever performed? Actually, does it even make sense to compare memory addresses for fault analysis? Additionally, even if these problems are overlooked, "performing substitute address allocation" is not found in the Tsukakoshi patent. Addresses are not substituted in the Tsukakoshi patent. That is, one memory address is not substituted for another, nor is the memory address for a defective memory location remapped to another memory location. The Tsukakoshi patent discloses using one bit of a FAM to represent multiple bits of a MUT. The MUT is not accessed at a later time, provided with a memory address for a first memory location that is remapped to a second memory location, or then accessed at the second memory location. The MUT is merely tested, a failure map is stored in the FAM, and then a redundancy solution is calculated. The Tsukakoshi patent does not discuss using the failure map in any way related to accessing the MUT, or substituting the failure map stored by the FAM for a memory address to be accessed.

The Examiner has characterized the Hancu article as teaching "algorithms 'A concurrent test architecture' wherein such techniques [of compressing memory addresses to reduce failure storage hardware] are described including error detection routine based on comparison of routing or address signatures in compressed format." *See* the Office Action p. 2. Ironically, the Hancu article describes a test architecture that includes *more* hardware than the conventional solution. For example, signature analyzers (SAs) need to be added at every node of the interconnection network of a multiprocessor system. *See* the Hancu article, p. 1171. Also, memory space is consumed by the need to store reference signatures to which the run time image is compared. *See id.* at p. 1169 and 1173. Even if it is not the case that additional hardware is needed for the system disclosed in the Hancu article, the address compression performed by the SAs is unsuitable for combination with the test mechanism of the Tsukakoshi patent. The compression performed by the SAs takes a source and/or destination address and provides a value that is passed to subsequent SAs in the program path until arriving at a destination for comparison to a reference signature. It is difficult to imagine how this process of address compression by SAs can be combined with the teachings of the Tsukakoshi patent, which "compresses" addresses by using one bit of a FAM to represent several bits of a MUT. No address values are stored in the Tsukakoshi patent, but instead, merely flags are stored in the FAM indicating that at least one bit of a group of bits in the MUT has failed. Exactly which bit

in the group has failed is not important, simply that one of the many has failed. Thus, the compression of the Hancu article has no relationship with the "address compression" of the Tsukakoshi patent.

As previously discussed, even if the Examiner's characterization of the Tsukakoshi patent and the Hancu reference were accurate, the combined teaching would fail to teach or suggest the combination of limitations recited by claim 41. For example, neither the Tsukakoshi patent or the Hancu article describe comparing a memory address of a memory access request to decompressed defective memory addresses that are otherwise stored in a compressed format. More specifically, memory access requests, let alone a memory address thereof, are not considered in either the Tsukakoshi patent or the Hancu article. Comparison to decompressed defective memory addresses is also not found in either the Tsukakoshi patent or the Hancu article. There is no mention of extracting a substitute address associated with the decompressed defective memory address when there is an address match. Furthermore, neither the Tsukakoshi patent or the Hancu article describes accessing a memory location corresponding to the extracted substitute address. None of the limitations are discussed in the Tsukakoshi patent because it is directed to a test system using a smaller FAM for storing the locations of defective memory locations of a MUT for the purpose of calculating a redundancy solution. No alternative memory locations are accessed, no addresses are compared. The Hancu article clearly fails to make up for any of the deficiencies of the Tsukakoshi patent because it is directed to a test architecture for a massively parallel computer.

For the foregoing reasons, claim 41 is patentable over the Tsukakoshi patent in view of the Hancu article. Therefore, the rejection of claim 41 under 35 U.S.C. 103(a) should be withdrawn.

The previous discussion with respect to the combined teachings of the Tsukakoshi patent and the Hancu article can be applied to claims 45, 49, 54, 59, and 64 as well. Claims 45, 49, 54, and 64 recite a respective combination of limitations that is neither taught nor suggested by the combined teachings of the Tsukakoshi patent and the Hancu article. Consequently, the rejection of claims 45, 49, 54, 59, and 64 under 35 U.S.C. 103(a) should also be withdrawn.

Similarly, claims 42-44, which depend from claim 41, claims 46-48, which depend from claim 45, claims 50-53, which depend from claim 49, claims 55-58, which depend

from claim 54, claims 60-63, which depend from claim 59, and claims 65-67, which depend from claim 64, are also patentable based on their dependency from an allowable base claim. That is, each of the dependent claims further narrow the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. However, because each claim in an application represents a different invention, the rejection of an independent claim does not necessarily result in the rejection of claims depending therefrom. For the foregoing reasons, the rejection of claims 42-44, 46-48, 50-53, 55-58, 60-63, and 65-67 under 35 U.S.C. 103(a) should also be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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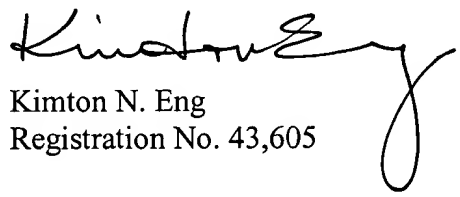

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